REMARKS

1. Claim Rejections – 35 U.S.C. 102(e)

Claims 1 – 4 and 6 – 8 were rejected under 35 U.S.C. 102(e) as being anticipated by Cho et al.

Response

Claim 1

Cho discloses a system decoder (Fig.3, Cho et al.) having an internal memory 280 and an internal memory controller 210, the system decoder being coupled to an A/V decoder by means of an A/V interface 120. Applicant states that the system in Claim 1 is not the same as the system disclosed by Cho et al. The system decoder of Cho is for performing demodulation and ECC decoding before data is transmitted to the A/V decoder for following audio and video data decoding: "An A/V decoder interface and DVD-ROM interface 120 transfers the descrambled data selectively to an A/V decoder and/or a ROM decoder according to the type of data stored on the DVD 100" [Col.5, lines 35 – 38]. Additionally, as depicted in Cho Fig. 3, the arrow symbol points out a one-way direction representative of a data outputting path to the external A/V decoder and/or the ROM decoder. The system of Claim 1, however, includes an ECC decoder circuit and a graphics decoding circuit that perform decoding utilizing the same memory controller and the same memory. That is, Claim 1 claims memory controller sharing and external memory sharing between the servo control and ECC decoder circuit and the graphics decoding circuit.

Furthermore, the memory disclosed in Claim 1 is an external memory, i.e. external to both the servo control and ECC decoder circuit and the graphics decoding circuit. It can be clearly seen from Fig.3 of Cho that the disclosed memory 280 is an internal memory of the system decoder, and only utilized by the system decoder 200. In other words, the memory 280, illustrated by Cho, cannot be utilized by a graphics decoding circuit as indicated in claims 1 and 12 because the memory 280 is only an internal memory for the system decoding purpose as shown in Fig. 3 of Cho. The applicant therefore asserts that

Cho does not teach 'storing the decoded data in an external memory', 'decoding graphics data held in the external memory to generate video data and audio data', and 'a memory controller to provide read and write access to the external memory for both the servo control and ECC decoder circuit and the graphics decoding circuit', as recited in Claim 1. Therefore, the applicant asserts that Claim 1 overcomes the rejection.

Claim 2

Claim 2 further defines that the graphics decoding circuit utilizes the memory controller for a write operation, i.e. storing video data in the external memory. As Cho does not disclose an external memory, and furthermore, does not disclose that a same memory controller is utilized by the A/V decoder and the system decoder, applicant asserts that Claim 2 overcomes the rejection. Furthermore, Claim 2 is dependent on Claim 1 and should be found allowable if Claim 1 is found allowable.

Claim 3

Claim 3 is dependent on Claim 1 and should therefore be found allowable if Claim 1 is found allowable.

Claim 4

Claim 4 discloses a communications pathway linking the servo control and ECC decoder circuit with the graphics decoding circuit. Cho discloses a communication path between the system decoder and the A/V interface. As Claim 4 discloses a system where there is a direct communication path between the servo control and ECC decoder circuit and graphics decoding circuit, the applicant asserts Claim 4 should be found allowable over the prior art. Furthermore, as Claim 4 is dependent on Claim 1 it should be found allowable if Claim 1 is found allowable.

2. Claim rejections – 35 U.S.C. 103(a)

Claim 9 was rejected under 35 U.S.C. 103(a) as being unpatentable over Cho in view of Chau and Haratsch et al.

Response

As Claim 9 is dependent on Claim 1, and the applicant believes that Claim 1 has

been placed in a position for allowance as per the arguments detailed in the response to Claim 1 above, Claim 9 should also be found allowable.

Claims 10 and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cho in view of Romano et al and Casalnuovo.

Response

Claim 10

Claim 10 is dependent on Claim 1 and should therefore be found allowable if Claim 1 is found allowable.

Claim 12

Claim 12 contains limitations of Claim 1, and further defines an electronic circuit fabricated on a monolithic substrate. As per the arguments detailed under the response to Claim 1, the applicant asserts that the Cho does not disclose a system where a servo control and ECC decoder circuit and a graphics decoding circuit perform decoding utilizing the same memory controller and an external memory. Furthermore, Cho fails to teach a direct communication path between the servo control and ECC decoder circuit and the graphics decoding circuit. Therefore, the combination of Cho with Romano and Casanuovo is unreasonable as such a combination would not result in the system of Claim 12. Therefore, applicant believes that Claim 12 should be found allowable.

Claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Cho in view of Washida et al and Yano et al.

Response

Claim 11 is dependent on Claim 1, and as applicant believes Claim 1 has been placed in a position for allowance, Claim 11 should also be found allowable.

Claims 15, 16, and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cho in view of Romano et al, Casalnuovo et al, Iwamura, and Kim et al.

Response

Claim 15

Claim 15 further defines limitations of how data is stored in the external memory. As per the arguments under the response to Claim 12, Cho does not disclose an external memory, and therefore the combination of Cho, Romano, and Casalnuovo would not result in the system of Claim 12, which Claim 15 is dependent on. Furthermore, Iwamura and Kim disclose a circular buffer for storing video data, but as the combination of Cho, Romano, and Casalnuovo does not result in a system with an external memory, applicant believes Claim 15 should overcome the rejection.

Claim 16

Claim 16 is dependent on Claim 15, which is itself dependent on Claim 12. As the applicant believes said claims have been placed in a position for allowance, Claim 16 should also be found allowable.

Claim 17

Claim 17 is also dependent on Claim 15, and should therefore be found allowable with reference to the arguments under response to claims 15 and 12.

Claims 5, 13, and 14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cho in view of Yuen et al.

Response

Claim 5

Yuen discloses a directory controller that indicates the location of video programs. As the applicant has already argued that Cho does not teach providing an external memory, the combination of Cho and Yuen would not result in the system disclosed in Claim 5. Furthermore, Claim 5 is dependent on Claim 1 and should be found allowable if Claim 1 is found allowable.

Claim 13

As per the arguments detailed above under the response to Claim 12, the system disclosed in Claim 12 is patentable over the prior art of Cho et al., and therefore utilizing the registers disclosed by Yuen in the prior art of Cho would not result in the system disclosed in Claim 13. Therefore, applicant believes that Claim 13 should be found

allowable over the prior art.

Claim 14

Claim 14 further defines the registers claimed in Claim 13. As Claim 14 is dependent on Claim 13, and applicant believes Claim 13 has been placed in a position for allowance, Claim 14 should also be found allowable.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)